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From: Kevin G. Shao, Reg. No. 45,095 Date: October 21, 2005

Operator: David Castro

Application No.: 09/471,637 Art Group: 2131

Filing Date: Dec. 23, 1999 Conf. No: 7753

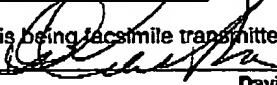
Entitled: PHYSICAL LAYER AND DATA LINK INTERFACE WITH ADAPTIVE SPEED

Attorney Docket No.: 42P7286

Enclosed are the following documents:

<input type="checkbox"/> Amendment/Response (<u> </u> pgs)	<input type="checkbox"/> Declaration & P of A (<u> </u> pgs)	<input type="checkbox"/> Reply Brief (<u> </u> pgs)
<input checked="" type="checkbox"/> Appellant's Reply Brief (<u> 5 </u> pgs)	<input type="checkbox"/> Drawings: <u> </u> # of sheets w/ <u> </u> figs.	<input type="checkbox"/> Small Entity Statement
<input type="checkbox"/> Utility Application (<u> </u> pgs)	<input type="checkbox"/> Month Petition re Ext. of Time	<input type="checkbox"/> Rsp. to Notice of Missing Parts (<u> </u> pgs)
<input type="checkbox"/> 1.53(b) Cont. Application (<u> </u> pgs)	<input type="checkbox"/> IDS & PTO 1449 (<u> </u> pgs)	<input type="checkbox"/> Transmittal Letter (<u> </u> pgs) (in duplicate)
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OCT 21 2005

Atty. Docket No. 42390.P7286

PATENTIN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:)	
)	
Yuval Bachrach)	Examiner: Laforgia C. A.
)	
Application No: 09/471,637)	Art Unit: 2131
)	
Filing Date: December 23, 1999)	Confirmation No.: 7753
)	
For: PHYSICAL LAYER AND DATA)	
LINK INTERFACE WITH)	
ADAPTIVE SPEED)	
)	

Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

APPELLANT'S REPLY BRIEF

Dear Sir:

Pursuant to 37 CFR §1.193, Appellant is filing this reply brief which addresses certain of the Examiner's points of argument which were raised in the Examiner's Answer. This reply brief is being submitted in triplicate.

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(Date of Deposit)David Castro
(Name of Person Mailing Correspondence)

(Signature)

Application No. 09/471,637

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Atty. Docket No. 42390.P7286

REMARKS

In response to Examiner's arguments that sections of col. 26, line 52 to col. 27, line 4; col. 28, lines 8-20; coo. 15, line 59 to col. 16, line 8; and col. 26, lines 26-65 of Boucher read on the limitations recited in claim 1 (see Examiner's answer, page 4), Appellant respectfully disagrees. It appears that newly cited sections of Boucher are different than those cited in the Final Office Action dated November 12, 2003 (see 11/12/2003 Office Action, pages 3-4).

Nevertheless, it is respectfully submitted that the present invention as claimed is related to packet communication between a physical layer (e.g., layer 1) and a MAC (media access control) layer (e.g., layer 2) of an OSI (open system interconnection) model of a network stack within a data processing system.

Specifically, for example as recited in independent claim 1, PHY-to-MAC words include slow mode PHY-to-MAC words received by the MAC layer (e.g., from layer 1 to layer 2) include a transmit cycle field to indicate whether the MAC provides data in a next MAC-to-PHY word from MAC to PHY (e.g., from layer 2 to layer 1). As a result, the speed of packet exchanges between MAC layer and PHY layer can be controlled by both layers via these kinds of communications. It is respectfully submitted that these limitations are absent from Boucher.

Rather, Boucher is related to whether to bypass the whole network stack. Specifically, for example, Boucher states:

“The INIC 150 has a network processor 170 which chooses between processing messages along a slow-path 158 that includes the protocol stack of the host, or along a fast-path 159 that bypasses the protocol stack of the host.”

(Boucher, Fig. 6, col. 10, lines 35 to 42, and emphasis added).

Thus, as shown in Fig. 6 of Boucher, hardware logic 171 or processor 170 (assuming physical layer or layer 1) determines whether the coming packets should be delivered via the fast path 159, which bypasses the network stack 152, including MAC or data link layer 160 (e.g., layer 2). Alternatively, the packets may be delivered via the slow path 158 using the whole network stack having layers 160-166. There is no mention of communications between the physical layer (e.g., processor 170 or hardware logic 171) and the MAC layer 160, particularly, using a transmit cycle field within the packets exchanged between the MAC layer and the PHY layer.

In response to Examiner's arguments that sections of col. 26, line 52 to col. 27, line 4; col. 28, lines 8-20; col. 15, line 59 to col. 16, line 8 of Boucher discloses the communications between PHY layer and MAC layer (see Examiner's answer, page 4), Appellant respectfully disagrees.

Although the cited sections mentions the words of PHY and MAC layers, there is no disclosure or suggestion within Boucher of communications between the PHY layer and the MAC layer using a transmit cycle field to adapt to various speeds as set forth above.

In order to anticipate a claim, each and every limitations of the claim must be taught by the cited references. It is respectfully submitted that Boucher fails to disclose each and every limitations set forth above. As a result, independent claim 1 is not anticipated by Boucher.

Similarly, independent claims 8 and 15 include limitations similar to those recited in claim 1. Thus, for the reasons similar to those set forth above, it is respectfully submitted that claims 8 and 15 are not anticipated by Boucher.

Given that the rest of the claims depend from one of the above independent claims, for the reasons similar to those set forth above, it is respectfully submitted that the rest of the claims are not anticipated by Boucher.

In response to Examiner's arguments regarding combining Boucher with U.S. Patent No. 4,525,795 of Rubin ("Rubin") and U.S. Patent No. 6,631,138 of Findlater et al. ("Findlater"), it is respectfully submitted that one with ordinary skill in the art, based on the teachings of the above references, would not combine with these references.

Specifically, Rubin is related to telephonic networking, particularly as shown in Fig. 2 of Rubin, between multiple computers instead of a network stack within a single computer system as described in Boucher. Further, Findlater is related to hardware pin interfaces between PHY and MAC (see Abstract of Findlater). The purpose of Findlater is to reduce a number of pins for the interfaces.

It is respectfully submitted that the above references solve significantly different problems and their approaches are significantly different. It is respectfully submitted that one with ordinary skill in the art, based on the teachings of the above references, would not combine with these references because such a combination lacks reasonable expectation of success. Such suggestions can only be found based on the impermissible hindsight of the present application.

Even if they were combined, for the reasons set forth above, such a combination still lacks the limitations set forth above. Therefore, it is respectfully submitted that claims 1-21 are patentable over the Boucher in view of Rubin and Findlater.

CONCLUSION

For the foregoing reasons, Appellant submits that all pending claims (1-21) are in condition for allowance. Appellant submits that all claims are patentable in light of Boucher, Rubin, and Findlater, and that the references either alone or in combination do not disclose, teach, or render obvious Appellant's claimed invention. Therefore, Appellant respectfully prays for reversal of the Examiner's rejections.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: October 21, 2005


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